REMARKS

Claims 1-23 are now present in this application.

Claims 1, 5, 10, 15, 16 and 18 have been amended, and claims 21-23 have been added. Reconsideration of the application, as amended, is respectfully requested.

Objection Under 37 CFR 1.75(c)

Claim 15 stands objected to under 37 CFR 1.75(c) as being of improper dependent form. In view of the foregoing amendments, it is respectfully submitted that this objection has been addressed. Reconsideration and withdrawal of any objection to the claims are respectfully requested.

Rejection Under 35 U.S.C. 112

Claims 15 and 16 stand rejected under 35 USC 112, first paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments, it is respectfully submitted that the claims would enable one of ordinary skill in the art to make and/or use the invention. Support for these amendments can be found on page 7 of the application. Specifically, the limitation "the non-active surface of the first chip exposed beyond the encapsulation remains exposed when the outer leads are attached to second level package" can be found on page 7, lines 22-27. It is therefore respectfully submitted that no new matter has been added. Reconsideration and withdrawal of the 35 USC 112, first paragraph rejection are respectfully requested.

Rejection Under 35 U.S.C. 102(e)

Claims 18 and 20 stand rejected under 35 U.S.C. 102(e) as being anticipated by Shim et al., U.S. Publication 2004/0061202. This rejection is respectfully traversed.

The Examiner asserts that "Shim discloses a second chip (30), having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads and an encapsulation (40) with the total wire non-connecting surface of the leads exposed beyond the encapsulation."

Independent claim 18 of the present application recites (emphasis added):

> 18. A dual chips stacked packaging structure, comprising:
> a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;
> a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;
> a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads and ***the second adhering surface of the chip paddle contacts the central area of the second chip***;
> a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and
> an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with ***the total wire non-connecting surface of the leads exposed beyond the encapsulation***.

It is clear that the dual chips stacked packaging structure in claim 18 comprises an encapsulation with **the total wire non-connecting surface of the leads exposed beyond the encapsulation, as shown in Fig. 7**. Besides, referring to the drawing of the specification, **the second adhering surface of the chip paddle contacts the central area of the second chip**.

However, as disclosed by Shim in paragraph [0037] and Fig. 1, "Lead fingers 16 include an outer portion 18 exterior of package 10, and ***inner portion 20 within package 10***."

In addition, Shim discloses in paragraph [0041] and Fig. 1 that the "Lower die/chip 26 is affixed to inner/center die pad 12 using die attachment (D/A) resin 28 and *upper die/chip 30 is affixed to outer ring die pad 14 using D/A resin 32*."

Referring to Shim, it is cleared that **this patent does not disclose that the second adhering surface of the chip paddle contacts the central area of the second chip, as recited in claim 18.** Moreover, referring to Fig. 1 in Shim, **the total wire non-connecting surface of the leads (the underside of the inner portions 20 of lead fingers 16) exist within package, but are not exposed beyond the encapsulation as shown in Fig. 7 of the present invention.**

In addition, Applicant notes in this regard that the MPEP instructs that "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." (MPEP 2131) That is, it is well established that patent descriptions do not define the precise proportions of the elements if the specification is completely silent on the issue. In other words, if the description of the specification can not be relied on, in combination with the drawings, for what they would not reasonably teach one of ordinary skill in the art.

It is therefore respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the structure of independent claim 18, or its dependent claims. Reconsideration and withdrawal of the 35 USC 102(e) rejection are respectfully requested.

Rejections Under 35 U.S.C. 103(a)

Claims 1-9 and 19

Claims 1-9 and 19 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al in view of Vaiyapuri et al., U.S. Patent 6,541,846. This rejection is respectfully traversed.

The Examiner asserts that "Shim does note expressly disclose the first and second chips adhering to either surface of the same parts of the chip paddle. However, Vaiyapuri discloses first (130)n and second (120) chips adhering to either surface of the same parts of the chip paddle (116)."a

It is noted that independent claims 1, 5, and 18 of the present application, recite:

> 1. A dual chips stacked packaging structure, comprising:
>
> a first chip, having an active surface and an opposing non-active surface, the active surface consisting of a central area and a peripheral area having a plurality of first bonding pads;
>
> a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, ***the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads***;
>
> a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, the active surface consisting of a central area and a peripheral area having a plurality of second bonding pads, ***wherein the first and second chips adhere to either surface of the center area of the chip paddle***; and
>
> a plurality of wires, wherein parts of the wires electrically connect with the first bonding pad and the leads, and parts of the wires electrically connect with

the second bonding pad and the leads.

5. A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;

a lead frame comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, ***the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads***;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads, ***wherein the first and second chips adhere to either surface of the center area of the chip paddle***;

a plurality of wires, parts of which electrically connect with the first bonding pad and the leads, and parts of which electrically connect with the second bonding pad and the leads; and

an encapsulation, covering the lead frame, the first chip, the second chip, and the wires.

18. A dual chips stacked packaging structure, comprising:

a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;

a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, ***the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads***, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;

a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads and ***the second adhering surface of the chip paddle contacts the central area of the second chip***;

a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and

an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with ***the total wire non-connecting surface of the leads exposed beyond the encapsulation***.

It is clear that the dual chips stacked packaging structure in claims 1, 5, and 18 comprise a first and a second chip, individually having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads. Besides, **the first and second chips adhere to either surface of the center area of the chip paddle**. In other words, the first adhering surface of the chip paddle adheres to the active surface of the first chip while the second adhering surface of the chip paddle connects with an opposing non-active surface of the second chip, **in such a way as to avoid contact with the first and second bonding pads**.

However, Shim et al. discloses in paragraph [0041] and Fig. 1 that the "Lower die/chip 26 is affixed to inner/center die pad 12 using die attachment (D/A) resin 28 and upper die/chip 30 is affixed to outer ring die pad 14 using D/A resin 32."

Vaiyapuri discloses in column 4, lines 54-61 and column 5, lines 3-12 that "A plurality of first dice 120 are attached to corresponding die attach surfaces 118 of die attach sites 116 on the first sides 112 of the base lead frames 110, as by conventional die pick and place equipment. Each first die 120 includes a back side 122 and an active surface 124 having substantially centrally located bond pads 126 in one or more rows or other arrangement on the active surface 124" and "A plurality of second dice 130 are attached to corresponding die attach surfaces 118 of die attach sites 116 on the second side 114 of the base lead frame 110. Each of the second dice 130 may be, but are not limited to, the same dimensions and the same type and configuration of semiconductor die the first dice 120. Each of the second dice 130 includes a back side 132 and

an active surface 134 having substantially centrally located bond pads 136 in one or more rows or other configuration on the active surface 134."

It is obvious that **neither Shim nor Vaiyapuri teaches that the first and second chips, consisting of a central area and a peripheral area having a plurality of first bonding pads, adhere to either surface of the center area of the chip paddle, as is recited in independent claims 1, 5, and 18 of the present application.** Moreover, neither citation discloses that **the adhering surface of the chip paddle adhering to the first and the second chips in a specific way is adapted to avoid contacting with the first and second bonding pads**. Specifically, Vaiyapuri does not recite that the chip paddle adheres to the first and the second chips in a specific way and the double down-set leadframe structure is well suited for die stacking,. Thus, the dual cips stacked packaging structure achieved by combining Shim et al. and Vaiyapuri would destroy the manufacturing principle of the present application.

The Examiner further asserts that "It would have been obvious for one skilled in the art at the time of the invention to align the chips of Shim as disclosed by Vaiyapuri, for the purpose of increasing the integrated circuit density of the semiconductor package device." However, as recited above, neither Shim nor Vaiyapuri teaches the adhering surface of the chip paddle adhering to the first and the second chips in a specific way to avoid contact with the first and second bonding pads.

Furthermore, MPEP 2142 states "The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness," and, "To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of

ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations."

It is respectfully submitted that the general benefits and advantages of the present invention include that the die attachment interface area is reduced; the packages are made more robust, i.e. there is less stress created at the die pads; there is lower stress in the die attachment interfaces; the packages are less sensitive to moisture adsorption; and the double down-set leadframe embodiments are well suited for die stacking. Thus, it can be seen that the motivation of manufacturing the dual chips stacked packaging structure by combining Shim in view of Vaiyapuri would be insufficient. Besides, combining Shim with Vaiyapuri cannot meet successful results, in other words, the method of combining Shim with Vaiyapuri cannot render the benefits of avoiding chip paddle contact with bonding pads, while the adhering surface of the chip paddle adheres to the first and the second chips. That is, the description or elements of the patent cannot be relied on, in combination with the drawings, for what they would not reasonably teach one of ordinary skill in the art. As discussed above, the structure of independent claims 1, 5, and 18, distinctly differs from the cited prior art.

In view of the foregoing amendments and remarks, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the structure of independent claims 1, 5 and 18, as well as their dependent claims. Reconsideration and withdrawal of the 35 USC 103 rejection are respectfully requested.

Claims 10-16

Claims 10-16 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Shim et al. in view of Wu et al., U.S. Publication 2003/0214048.

The Examiner asserts that "Shim does note expressly disclose the non-active surface (351) of a first chip (35) being exposed from the encapsulation."

Independent claim 10 recites:

> 10. A dual chips stacked packaging structure, comprising:
> a first chip, having an active surface and an opposing non-active surface, wherein the active surface consists of a central area and a peripheral area having a plurality of first bonding pads;
> a lead frame, comprising a plurality of leads and a chip paddle having a first adhering surface and a second adhering surface, the first adhering surface adhered to the active surface of the first chip in such a way as to avoid contact with the first bonding pads, and each of the leads comprising a wire connecting surface and an opposing wire non-connecting surface;
> a second chip, having an active surface and an opposing non-active surface connecting with the second adhering surface of the chip paddle, wherein the active surface consists of a central area and a peripheral area having a plurality of second bonding pads, ***wherein the first and second chips adhere to either surface of the center area of the chip paddle***;
> a plurality of wires, parts of which electrically connect with the first bonding pad and the wire connecting surface of the leads, and parts of which electrically connect with the second bonding pad and the wire connecting surface of the leads; and
> an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the non-active surface of the first chip and the total wire non-connecting surface of the leads exposed beyond the encapsulation.
> an encapsulation, covering the chip paddle, the second chip, the wire connecting surface of the leads, the active surface of the first chip, and the wires, with the total wire non-connecting surface of the leads exposed beyond the encapsulation.

It is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest a dual chips stacked packaging structure, ***wherein the first and second chips adhere to***

either surface of the center area of the chip paddle, as required in independent claim 10 of the present application. Accordingly, it is respectfully submitted that the prior art utilized by the Examiner fails to teach or suggest the structure of independent claim 10, as well as its dependent claims. Reconsideration and withdrawal of the 35 USC 103 rejection are respectfully requested.

Newly Presented Claims

Applicant has added claims 21-23 and respectfully asserts that support for these claims can be found, for example, on pages 7-8 and FIG. 8 of the originally filed application. Accordingly, it is respectfully submitted that no new matter is introduced.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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